IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

MARCUS KUEGLER ET AL

Atty. Docket

CH 000007

Serial No.

Filed: CONCURRENTLY

A METHOD AND APPARATUS FOR TESTING DIGITAL CIRCUITRY

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Prior to calculation of the filing fee and examination, please amend the above-identified application as follows:

IN THE CLAIMS

Please amend the claims as follows:

4. (Amended) A method as claimed in Claims 1, whilst in connection with said buffering executing a conversion between a digital full swing internal signal and an analog low swing external signal with respect to core circuitry of said digital circuitry.

5. (Amended) A method as claimed in Claims 1, whilst controlling both said loop-back as well as said buffering through a one-bit control signal.

10. (Amended) An apparatus as claimed in Claims 7, provided with conversion means for in connection with said buffering executing a conversion between a digital full swing internal signal and an analog low swing external signal with respect to core circuitry of said digital circuitry.

11. (Amended) An apparatus as claimed in Claims 7, wherein both said loop-back as well as said buffering have a one-bit control signal input.

REMARKS

The claims have been amended in order to reformat the claims to delete all multiple dependencies prior to calculation of the filing fee and place the instant application in standard U.S. format.

Entry of this amendment prior to calculating the filing fee is respectfully requested.

Respectfully submitted,

By_____
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April 3, 2001

APPENDIX

4. (Amended) A method as claimed in Claims 1, ~~2 or 3,~~ whilst in connection with said buffering executing a conversion between a digital full swing internal signal and an analog low swing external signal with respect to core circuitry of said digital circuitry.

5. (Amended) A method as claimed in Claims 1, ~~2 or 3,~~ whilst controlling both said loop-back as well as said buffering through a one-bit control signal.

10. (Amended) An apparatus as claimed in Claims 7, ~~8 or 9,~~ provided with conversion means for in connection with said buffering executing a conversion between a digital full swing internal signal and an analog low swing external signal with respect to core circuitry of said digital circuitry.

11. (Amended) An apparatus as claimed in Claims 7, ~~8 or 9,~~ wherein both said loop-back as well as said buffering have a one-bit control signal input.